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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
VOCKRODT, JEFF B

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

A-A

Office Action Summary	Application No.	Applicant(s)	
	09/160,657	LYDING ET AL.	
	Examiner	Art Unit	
	Jeff Vockrodt	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40-48 and 60-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *40-48 and 60-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *40* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the IDS filed February 10, 2003. Claims 40-48 & 60-81 are pending. The most recent amendment that has been entered was filed on June 12, 2002.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 66-70 and 72-73 are rejected under 35 U.S.C. 102(b) as being anticipated by P.C.T. International Application WO 94/19829 ("Lisenker").

Lisenker teaches annealing a MOS gate in a deuterium containing atmosphere and a polysilicon layer is formed by CVD employing deuterium containing compounds (abstract). The device is subsequently cleaned using deuterium containing compounds (abstract). Lisenker preferably uses 0.99 mole fraction deuterium annealing atmosphere (page 9). In preferred embodiments, the ratio of deuterated to hydrogenated silicon bonds is 99:1 (page 11). Lisenker is concerned with stabilizing gate threshold voltage (page 6) and acknowledges problems in MOS devices such as "high sensitivity to hot carrier degradation." Claim 66 calls for greater than 10^{16} atoms/cc deuterium at the oxide/silicon interface and Lisenker does not report the concentration of deuterium at the oxide-silicon interface of the MOS gate.

Claim 66 covers devices having a deuterium concentration greater than 10^{16} atoms/cc--a value that one of ordinary skill in the art would regard as "almost no deuterium incorporated into the device." In Ference, the anneal example C (Fig. 4) has a concentration of deuterium in the gate oxide layer greater than 2×10^{16} atoms/cc. Ference characterizes this as "almost no

deuterium." (Ference, page 749, col. 1.) Such a low deuterium level is achieved by using a nitride blocking layer, which is not present in Lisenker. In contrast, the other examples A and B, which are more like Lisenker than example C, teach deuterium at concentrations that are two magnitudes higher than the claimed minimum concentration. The aim of Lisenker is to increase the amount of deuterium at the gate oxide interface and there is nothing to suggest that Lisenker utterly fails to meet its purpose by forming devices that have almost no deuterium incorporated into the device. Based on this evidence, and all the evidence of record, it is more likely than not that Lisenker necessarily results in a device having greater than 10^{16} atoms/cc of deuterium at the interface between the gate oxide and the silicon. Even if an amount of deuterium was driven out of the mos device of Lisenker during subsequent contacts that reduces the level of deuterium below the required amount, claim 66 would still be anticipated because it reads on the intermediate product that is formed before any contacts might be made to the device (i.e., before any deuterium might be driven out of the device). Accordingly, Lisenker anticipates claim 66.

Claim 67. Claim 4 of Lisenker teaches a polysilicon gate.

Claim 68. Lisenker teaches a silicon oxide gate dielectric (Fig. 1).

Claim 69. Polysilicon is polycrystalline silicon (does this further limit claim 66?).

Claim 70. The film is a gate dielectric.

Claim 72. The substrate is silicon (Fig. 1).

Claim 73. A doped region (source or drain) is a necessary component of a MOS device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject

matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 40-48, 60-65, and 75-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,514,628 ("Enomoto") in view of P.C.T. International Application WO 94/19829 ("Lisenker").

Lisenker teaches that where hydrogen is used to remove dangling bonds at the Si/SiO_2 interface in transistor gate oxides, page 2, ll. 10-25, substitution of hydrogen with deuterium results in transistors having improved stability, quality, and reliability, page 4, ll. 32-34. Lisenker, in discussing the many ways in which deuterium can be substituted for hydrogen, states that, "an annealing step is conducted in a deuterium atmosphere instead of a hydrogen atmosphere," pp. 5, ll. 5-15. Thus, Lisenker suggests improving hydrogen anneal passivation steps, by substituting deuterium for hydrogen as an annealing gas in passivation processes.

Of the hydrogen annealing examples taught by Lisenker, there is no mention of a hydrogen annealing step occurring after electrical contacts are formed on a semiconductor device. Therefore, Lisenker alone does not teach a deuterium annealing step that occurs after electrical contacts have been formed over a semiconductor device.

Enomoto teaches a two step sinter (anneal) post metal hydrogen passivation method whereby a sufficient sinter operation is preceded by an insufficient sinter operation and a testing step. In discussing the background of the invention, Enomoto states that hydrogen anneal processes, "typically [occur] toward the end of the fabrication process," col. 1, ll. 59-62. In the preferred embodiment, the final and sufficient sinter step is carried out in a hydrogen atmosphere at a temperature of approximately 400°C for more than 30 minutes after forming electrical contacts, col. 3, ll. 30 & col. 4, ll. 25-35. The sufficient sinter step reduces interface traps by terminating dangling bonds with hydrogen.

Lisenker and Enomoto are analogous art. Both references teach reducing interface states in semiconductor devices to increase device reliability and performance by way of passivation.

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the hydrogen of the post metallization anneal step in Enomoto, with deuterium, as suggested by Lisenker. The motivation to combine references in this manner comes from Lisenker's teaching that deuterium is superior to hydrogen for increasing device quality and reliability, and that deuterium can be substituted for hydrogen in passivation processes.

In re claims 41, 60-61, and 63, the gate material is preferably silicon oxide.

In re claim 42 and 64, the silicon semiconductor layer is single crystal which is referred to in reference to the underlying crystal structure.

In re claim 43 and 75-78, Enomoto teaches that the sufficient sinter step (anneal) can last 30-60 minutes.

In re claim 44, Lisenker teach a silicon wafer (abstract) which in its ordinary usage implies a single crystal silicon wafer.

In re claims 45 and 75-78, Lisenker at page 1 incorporates by reference the article Sah, "Models and Experiments on Degradation of Oxidized Silicon", Solid-State Electronics, vol. 33, pp. 147-167. The Sah article at page 160 teaches a forming gas composition of 10% hydrogen and 90% nitrogen which is used for device passivation.

In re claim 46, figure 1 of Lisenker reference shows deuterium and hydrogen covalently bonded to silicon.

In re claim 47, the chip is subsequently packaged, Enomoto, col. 2, ll. 2-3.

In re claim 48 and 65, the existence of covalently bonded deuterium is suggested in the above combination, and shown by figure 1 of Lisenker.

In re claims 62-65 and 75-78, claim 62 Enomoto teaches a preferred temperature of 400°C, abstract.

Claims 40-48, 60-65, and 75-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazaki et al., "Characteristics of Sub-1/4-μm Gate Surface Channel PMOSFET's Using a Multilayer Gate Structure of Boron-Doped Poly-Si on Thin Nitrogen-Doped Poly-Si," IEEE Transactions of Electron Devices, Vol. 41, No. 12, December 1994, pp. 2369-2375 ("Okazaki") in view of U.S. Pat. No. 5,864,161 ("Mitani") and P.C.T. International Application WO 94/19829 ("Lisenker").

Okazaki teaches a MOS transistor having a gate oxide of 3.5 nm (35 Angstroms) and 5 nm (50 Angstroms) (see e.g. Okazaki, page 2370, 1st full paragraph) that is susceptible to hot carrier degradation (see e.g. Okazaki, page 2372, 2d col.). Okazaki acknowledges the trend of decreasing gate oxide thickness in deep submicrometer CMOS (see Okazaki, page 2369, "Introduction").

Mitani teaches a p-channel MOS transistor (Third Embodiment, col. 22) formed by a method comprising the steps of forming on a semiconductor substrate a gate oxide 203 (Fig. 21A) having a thickness of 10 nm (100 Angstroms) (col. 22, ll. 17-18); forming a gate stack, an oxide over the gate stack having contact holes, and contacts 214 (Fig. 21E); and performing an anneal in nitrogen containing 10% hydrogen at 450°C for 15 minutes, thereby completing an MOS transistor. Mitani establishes that post-contact anneals in hydrogen were well known and desirable for MOS transistors useful for CMOS applications.

Lisenker, as discussed previously in relation to claims 40-48, 60-65, and 75-78, teaches substituting deuterium for hydrogen in processes such as hydrogen anneals to reduce device degradation due to hot carrier stress.

Okazaki, Mitani, and Lisenker are analogous art because they are within the field of CMOS devices and relate to the problem of hot-carrier reliability.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the post-contact anneal of Mitani modified to include deuterium in the transistor of Okazaki having a gate oxide of less than 55 angstroms. One of ordinary skill in the art would have been motivated to make these modifications by the expectation of improved hot carrier reliability as taught by Lisenker.

Claims 71 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lisenker in view of Mitani.

Lisenker anticipates claims 66-70 and 72-73 as discussed above.

Claims 71 and 74 depend from claim 66 and further require CMOS and spacers or field oxide respectively. Mitani teaches CMOS using spacer and field oxides (See e.g. Fig. 39R) and further includes hydrogen anneals. Mitani and Lisenker are analogous art. It would have been obvious to one of ordinary skill in the art at the time of the invention to use CMOS, spacers, or field oxide with the MOS device of Lisenker, since these devices were well known and desirable implementations or MOS devices as taught by Mitani.

Rejection of Claim Corresponding to Proposed Count

Claims 66-74 of this application have been copied by the applicants from U. S. Patent No. 6,023,093. These claim are not patentable to the applicants as set forth above.

An interference cannot be initiated since a prerequisite for interference under 37 CFR 1.606 is that at least one claim subject to a judgment in the interference be patentable to the applicants

Response to Arguments

Applicants' arguments filed June 12, 2002 have been fully considered but they are not persuasive.

As a result of the interview on April 10, 2003, the rejection based on Saks has been withdrawn and the rejection of claims 66-74 under 112 1st paragraph is withdrawn. Applicant's proposed amendments from the interview have not actually been filed so the examiner has no occasion to decide them at this time.

The examiner withdrew Saks because Saks does not address hot carrier degradation and is of little relevance in addressing the patentability of the claims since it is unrelated to the problems of hot carrier effect that are addressed by applicant. Lisenker is much more pertinent to the claimed invention since it addresses problems of hot carrier effect that occurs devices having reduced dimensions (the gate dielectric of Saks is much thicker than that of the devices pertinent to the claimed invention). While applicant appears to agree with this contention, it must be noted that any teaching away that could be attributed to Saks is correspondingly reduced by the fact that Saks is irrelevant to the obviousness analysis. One of ordinary skill in the art looking at the closest reference of record--Lisenker--would not have been dissuaded from applying Lisenker in the manner asserted in the ground of rejection by the older, irrelevant teaching of Saks.

Applicant has contended that the examiner is taking Lisenker out of context. The examiner disagrees. Statements in Lisenker such as: "The present invention can be implemented throughout the VLSI fabrication procedure. A typical fabrication procedure will include various doping, etching, annealing, deposition, cleaning, passivation, and oxidation steps. In each instance in which hydrogen or a hydrogen containing compound is employed, deuterium or a deuterium containing compound can be used in its place" (page 8)

unambiguously suggest that Lisenker can be combined with processes that use hydrogen beyond those that occur before interconnects are made.

Applicant has asked the examiner to compare the isotope effect between their application and the prior art (Lisenker). The examiner has made out a prima facie case of obviousness, the burden of production is on applicant. At any rate, the examiner is unable to make a comparison between the claimed invention and Lisenker that would be based on sufficient facts or data, since Lisenker does not report the results in terms of transconductance degradation as does applicant. Applicant may wish to make a specific comparison and present it to the examiner to consider in the next response--the examiner is unaware of how this can be done reliably and thus cannot perform the comparison in the first instance. A comparison with Saks would not be helpful to the obviousness analysis since it is not the closest prior art and is largely irrelevant. The only comparison made by the specification is the use of deuterium versus hydrogen (it is not even clear whether the results are for pre- or post- annealed devices), but the use of deuterium versus hydrogen is old (See Lisenker). Accordingly, the obviousness rejections stand.

Conclusion

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

J. Vockrodt
May 1, 2003

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